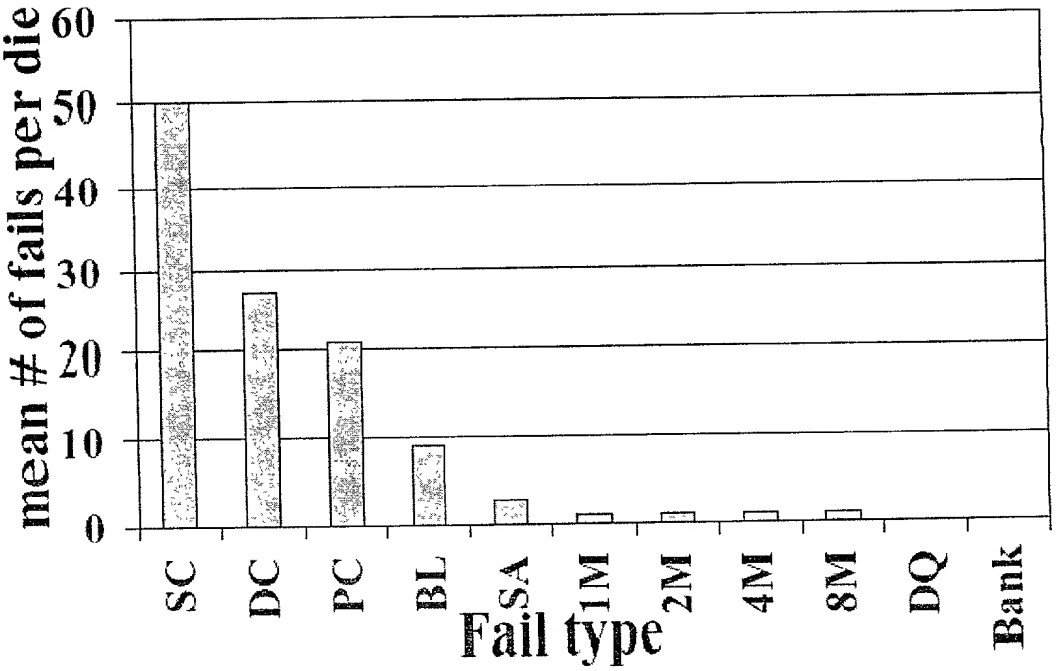
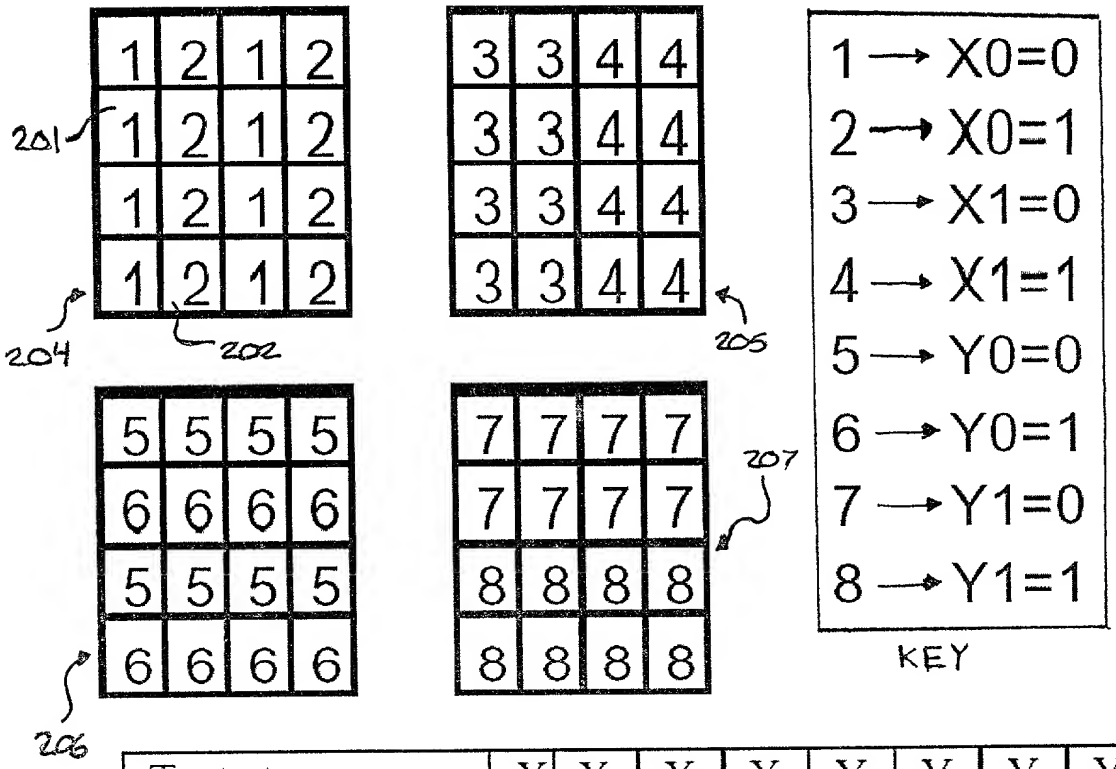

mean # of fails per die
60
50
40
30
20
10
0
SC
DC
PC
BL
SA
1M
2M
4M
8M
DQ
Bank
Fail type

Fig. 1



Test step	X 0 = 0	X 0 = 1	X 1 = 0	X 1 = 1	Y 0 = 0	Y 0 = 1	Y 1 = 0	Y 1 = 1
Chip	.	F	F	.	.	F	.	F

200

Fig. 2

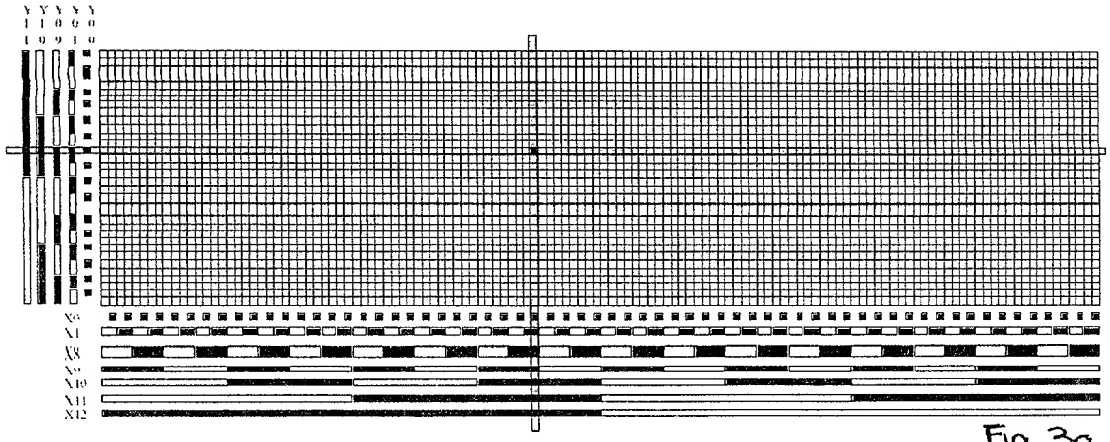


Fig. 3a

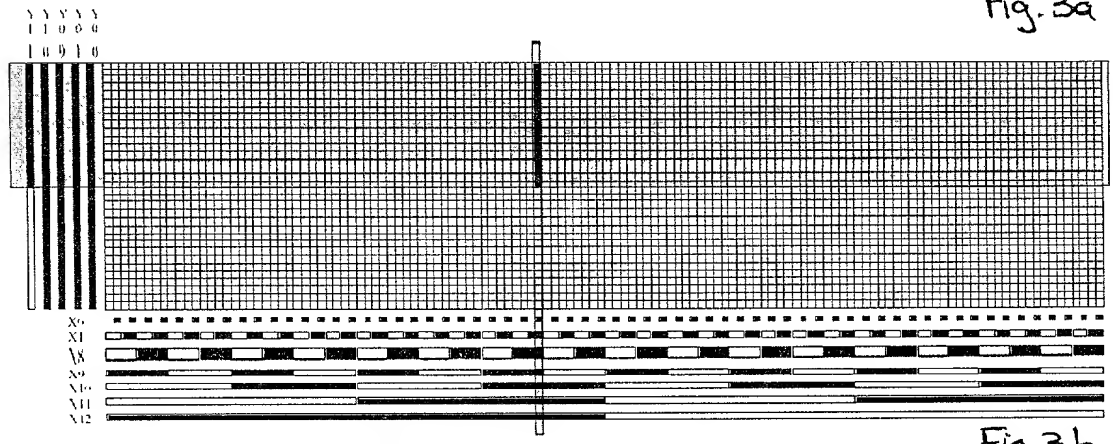


Fig. 3b

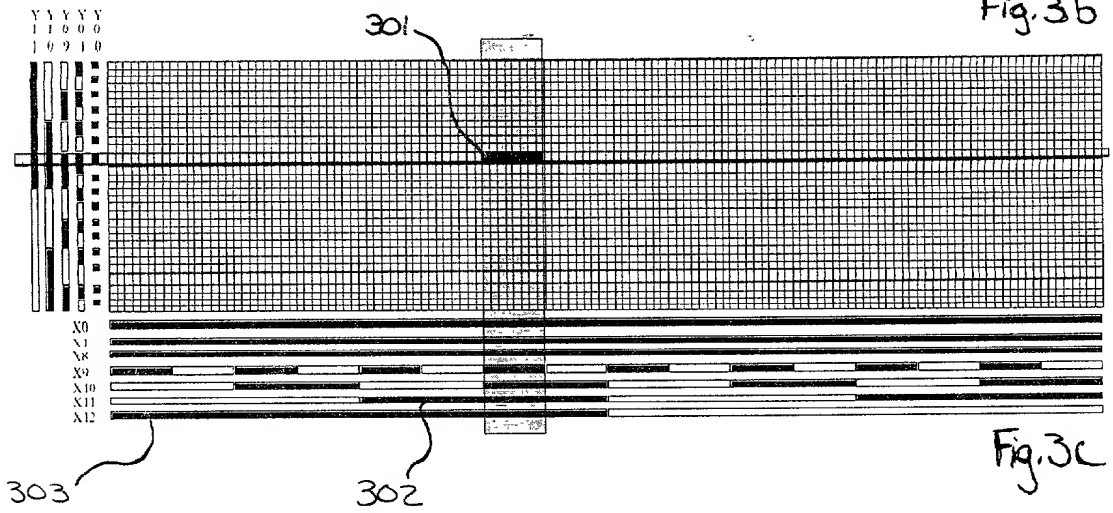


Fig. 3c

1	2	1	2
3	4	3	4
1	2	1	2
3	4	3	4

5	5	6	6
5	5	6	6
7	7	8	8
7	7	8	8

1 x0=0,y0=0
2 x0=1,y0=0
3 x0=0,y0=1
4 x0=1,y0=1

5 x1=0,y1=0
6 x1=0,y1=1
7 x1=1,y1=0
8 x1=1,y1=1

Fig. 4

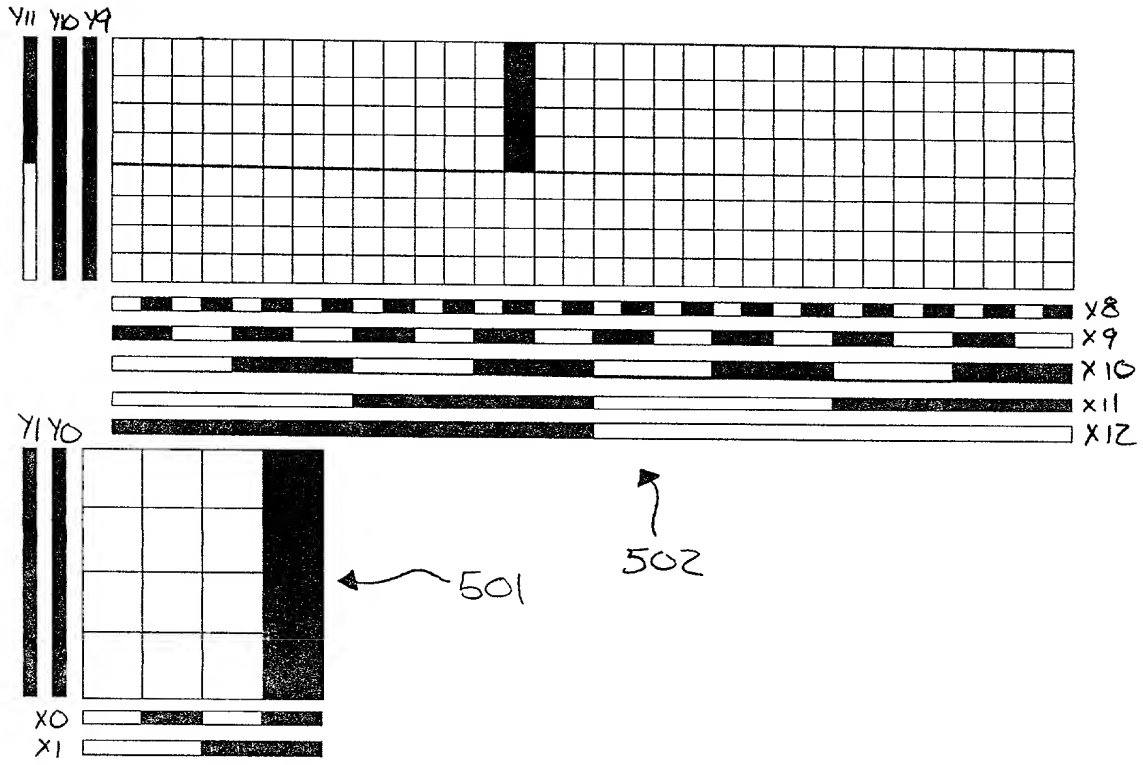

Y11 Y10 Y9
X8
X9
X10
X11
X12
Y1 Y0
X0
X1
501
502

Fig. 5

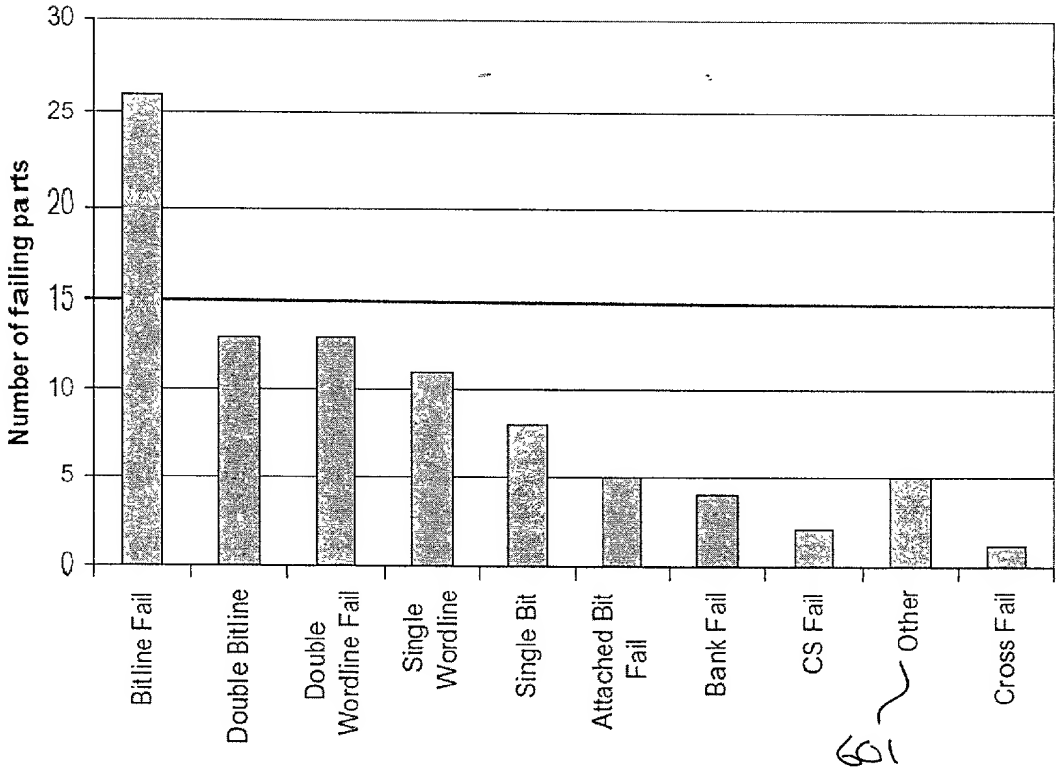
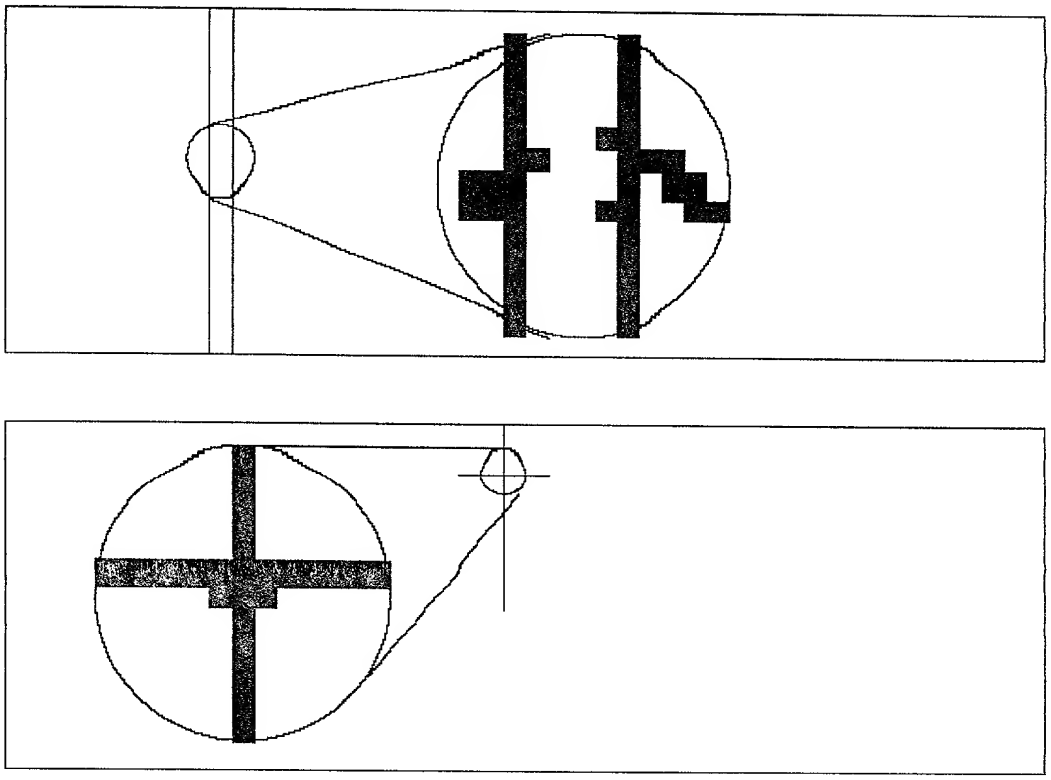

Number of failing parts
30
25
20
15
10
5
0
Bitline Fail
Double Bitline
Double Wordline Fail
Single Wordline
Single Bit
Attached Bit Fail
Bank Fail
CS Fail
Other
Cross Fail
601

Fig. 6

256k SRAM 139 145



246

Fig. 7

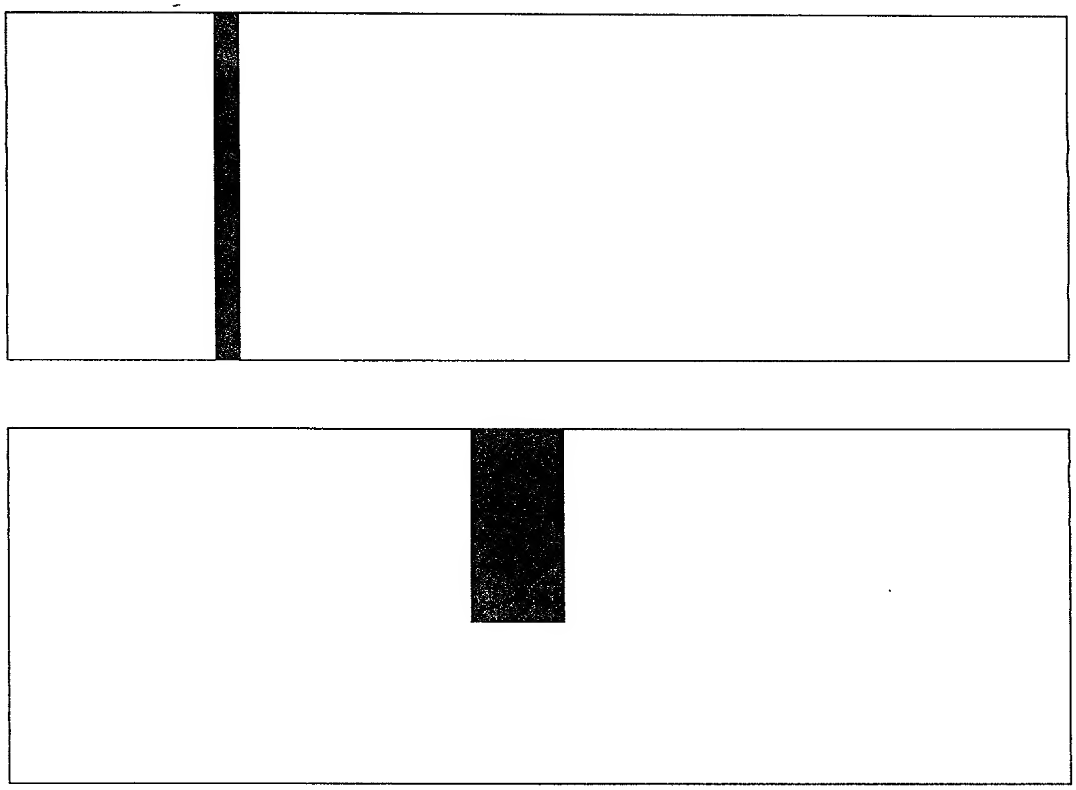


Fig. 8

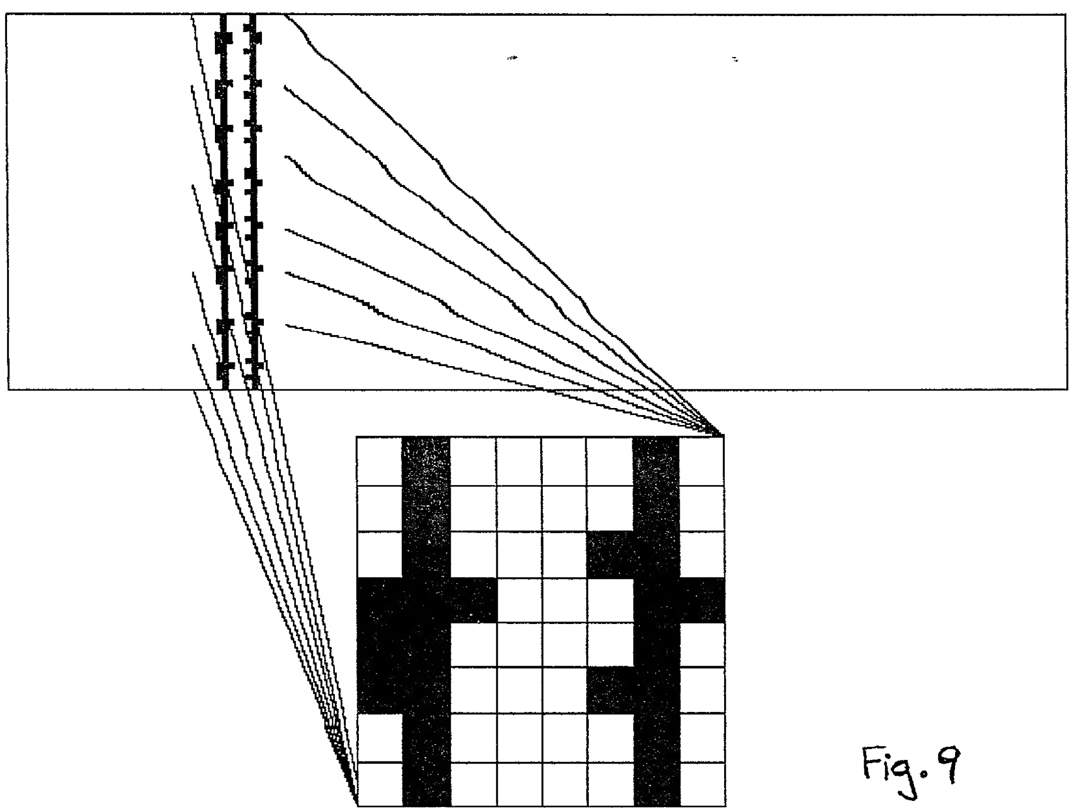


Fig. 9

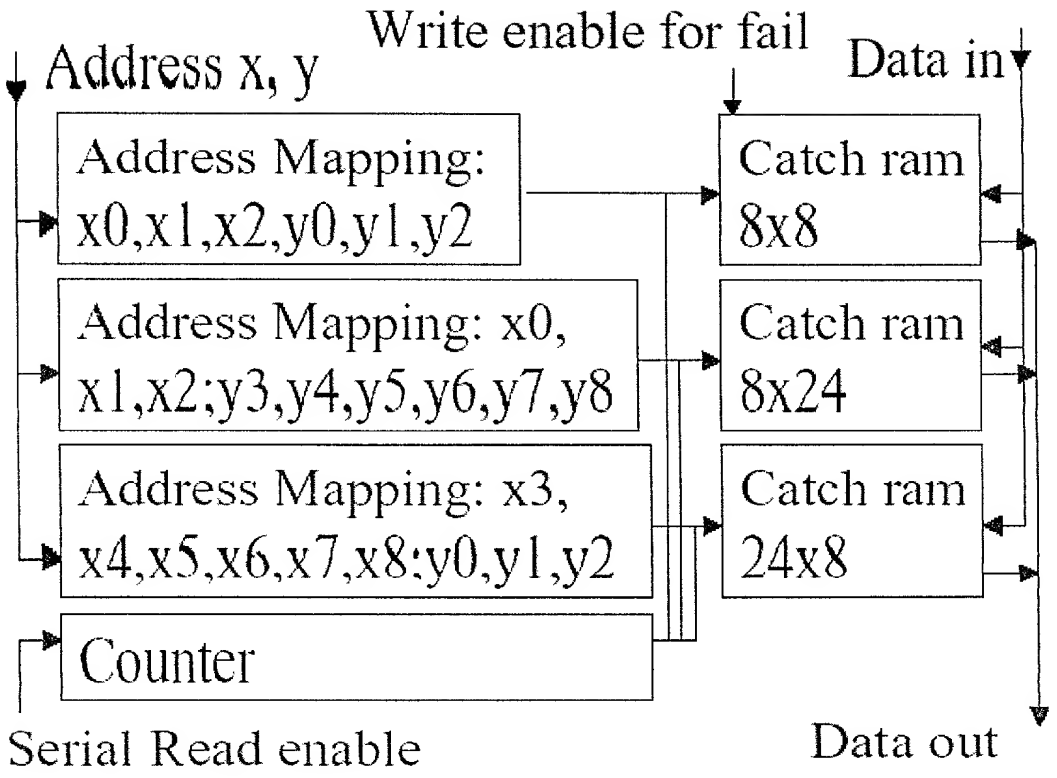

Write enable for fail
Address x, y
Data in
Address Mapping:
x0,x1,x2,y0,y1,y2
Catch ram
8x8
Address Mapping: x0,
x1,x2;y3,y4,y5,y6,y7,y8
Catch ram
8x24
Address Mapping: x3,
x4,x5,x6,x7,x8;y0,y1,y2
Catch ram
24x8
Counter
Serial Read enable
Data out

Fig. 10

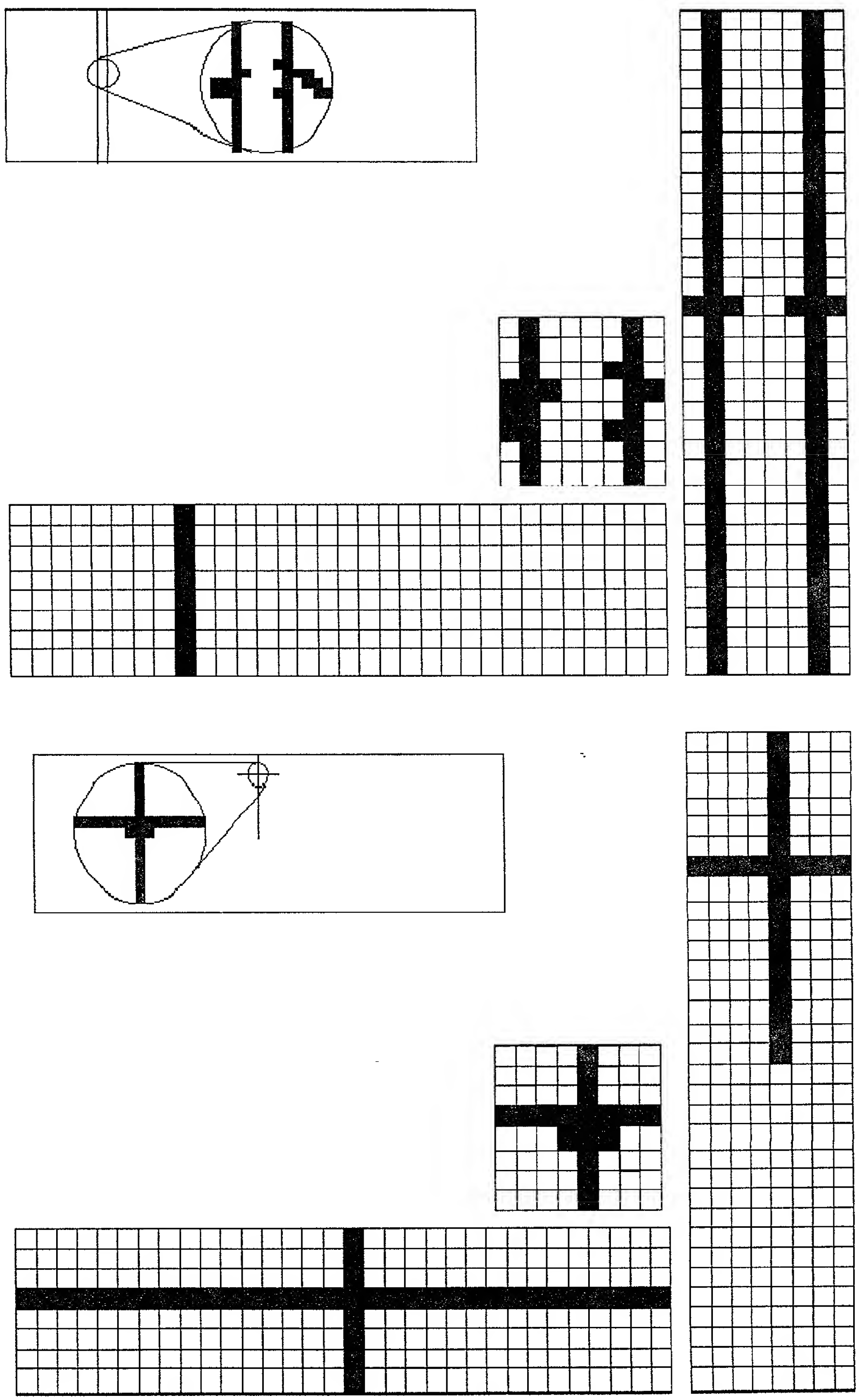


Fig. 11

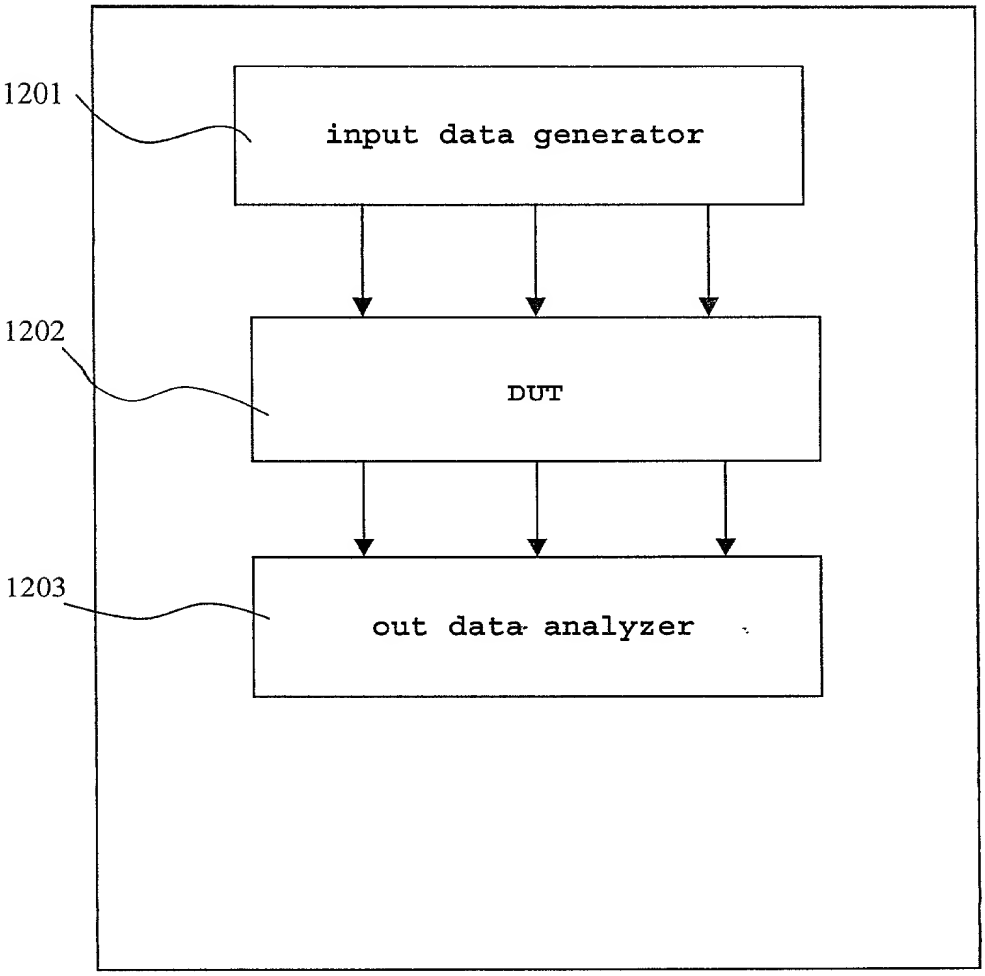


Fig. 12

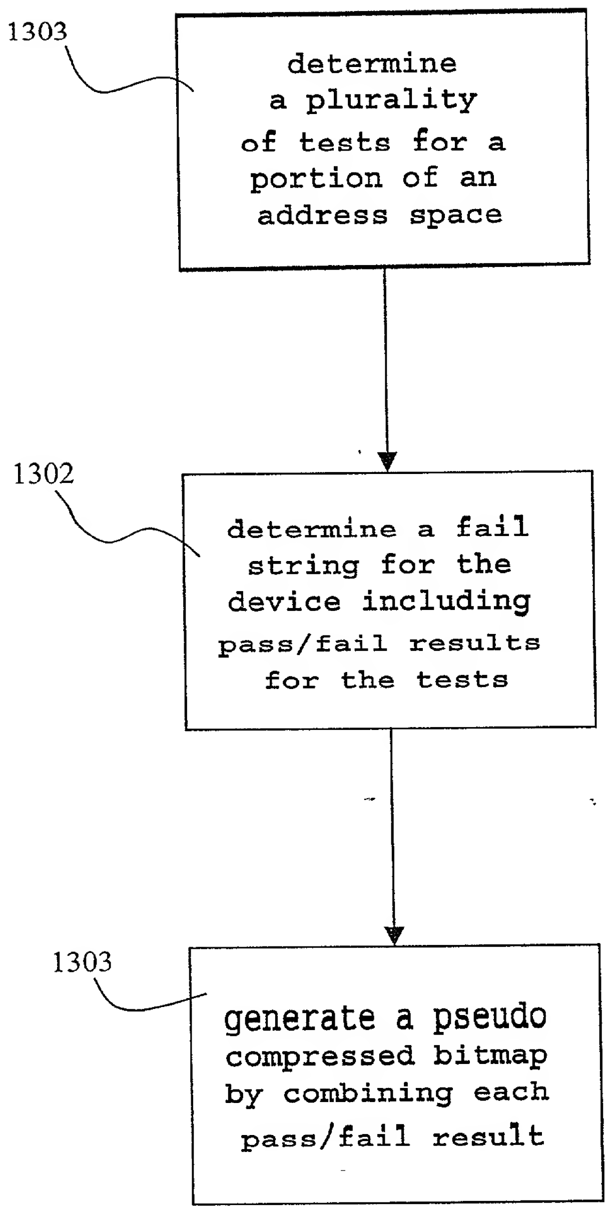


Fig. 13